Lab 10: Brandon Kowal, Bernard Owusu Sefah

Latches and Flip-Flops

Abstract

The lab has us design and test Latches and Flip-Flops using WinLogiLab. Making the D latch than the master-slave D flip-flop helps us understand how the latches work and the positive edge-triggered D Flip-Flop works. Working on the ETS-7000 made the wiring process easy to understand better than we did while using winlogi.

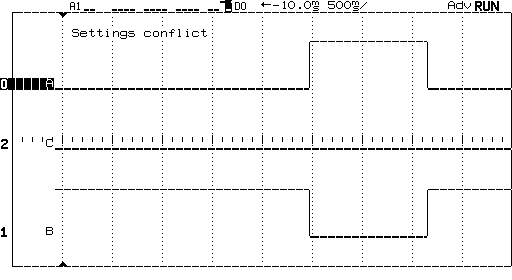
Introduction

This lab helps us understand how to design and test latches and flip-flops. The lab will have us design a SR and D latches, Master-Slave D flip-flop, and a positive edge-triggered D flip-flop. Using WinLogiLab to test these circuits.

Methods

1. We developed an SR latch circuit using winlogi data simulation and captured the timing diagram and tested the circuit’s functionality.
2. We used winlogi lab data simulation to develop a D-latch circuit and tested the validity using the truth table provided on the lab manual.
3. Using the previously D-latch design, we developed a master and slave latch which also validates the truth table which was provided in the lab manual.
4. We then wired the master and slave D-latch on the ETS-7000, tested the validity and the displayed the results on the MSO.
5. We then captured the results which was outputted by the master and slave D-latch from the MSO and save it on a flash drive.
6. Finally, we then had to design and construct a positive edge trigger on the ETS-7000 using similar design as the master and slave D-latch which was controlled by Pa and Pb on the ETS-7000 to display output results through the led.

Results

Fig 1 Master and slave D-Latch on MSO

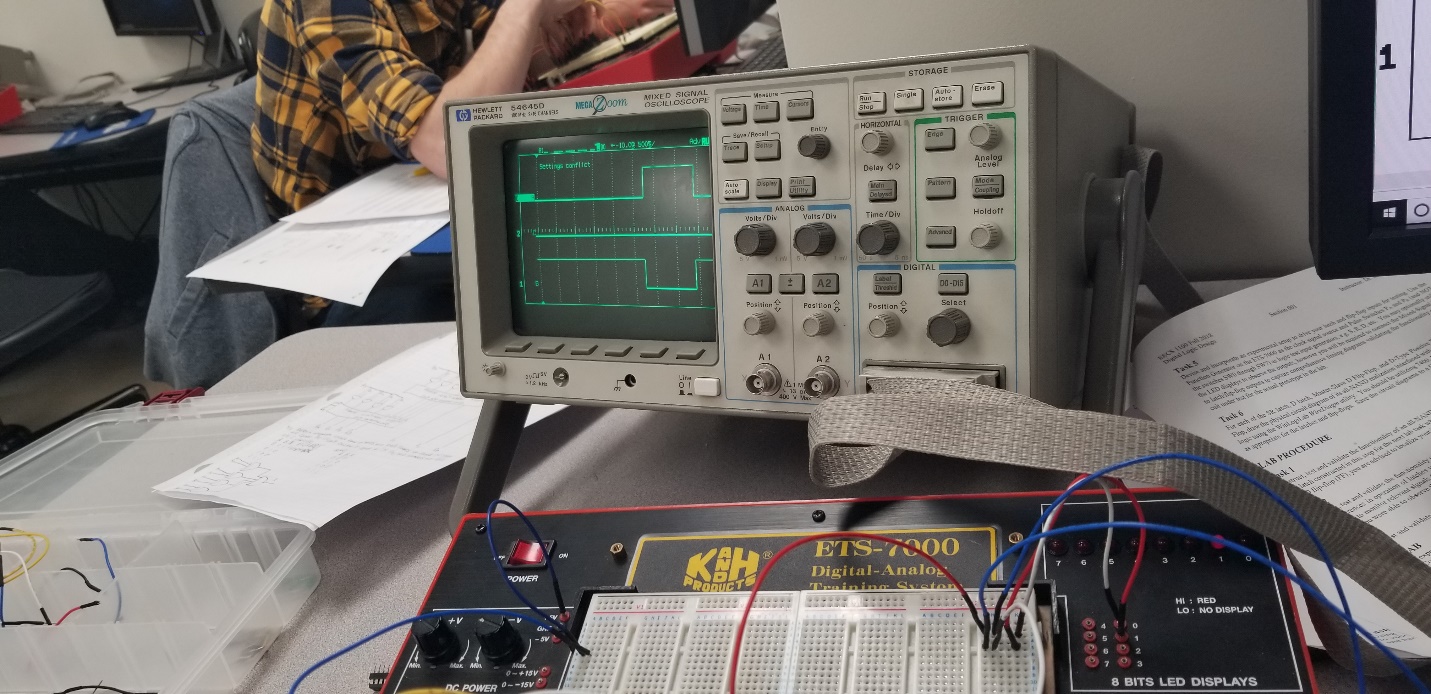
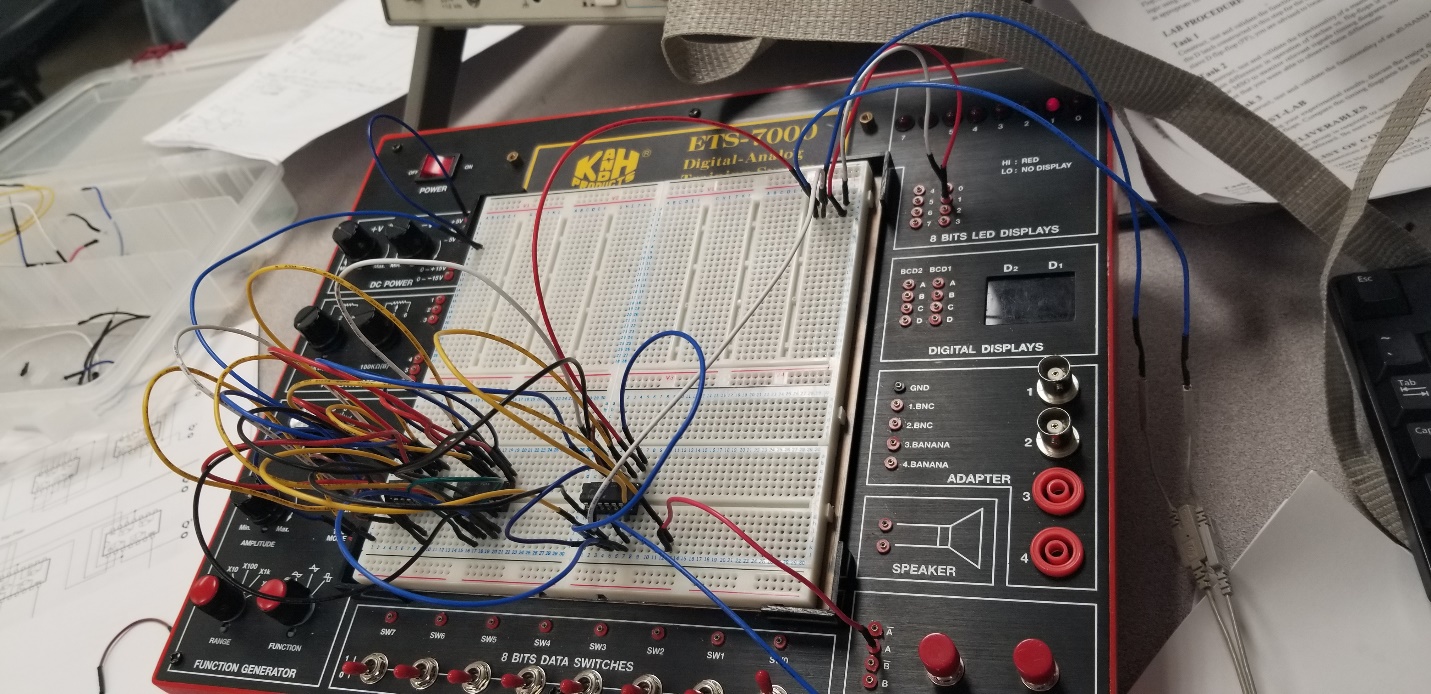


Fig 2 D-type Positive Edge trigger

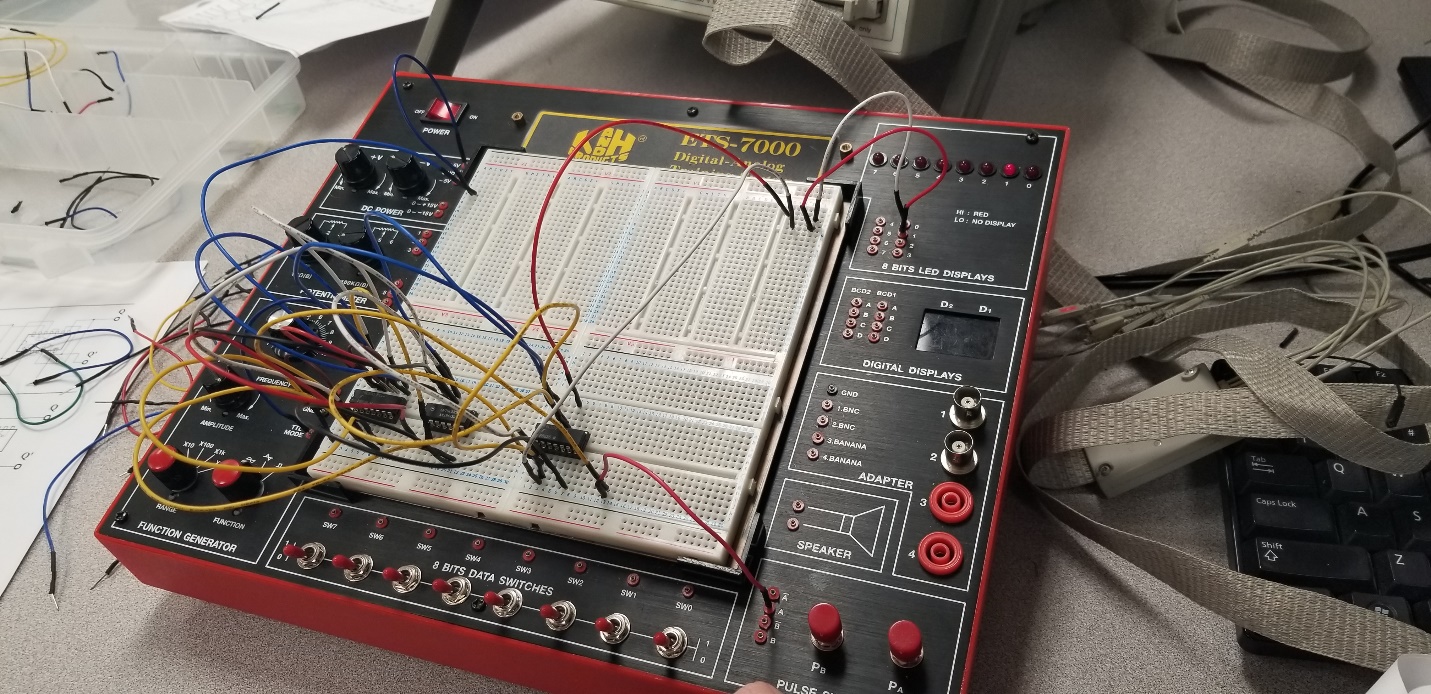
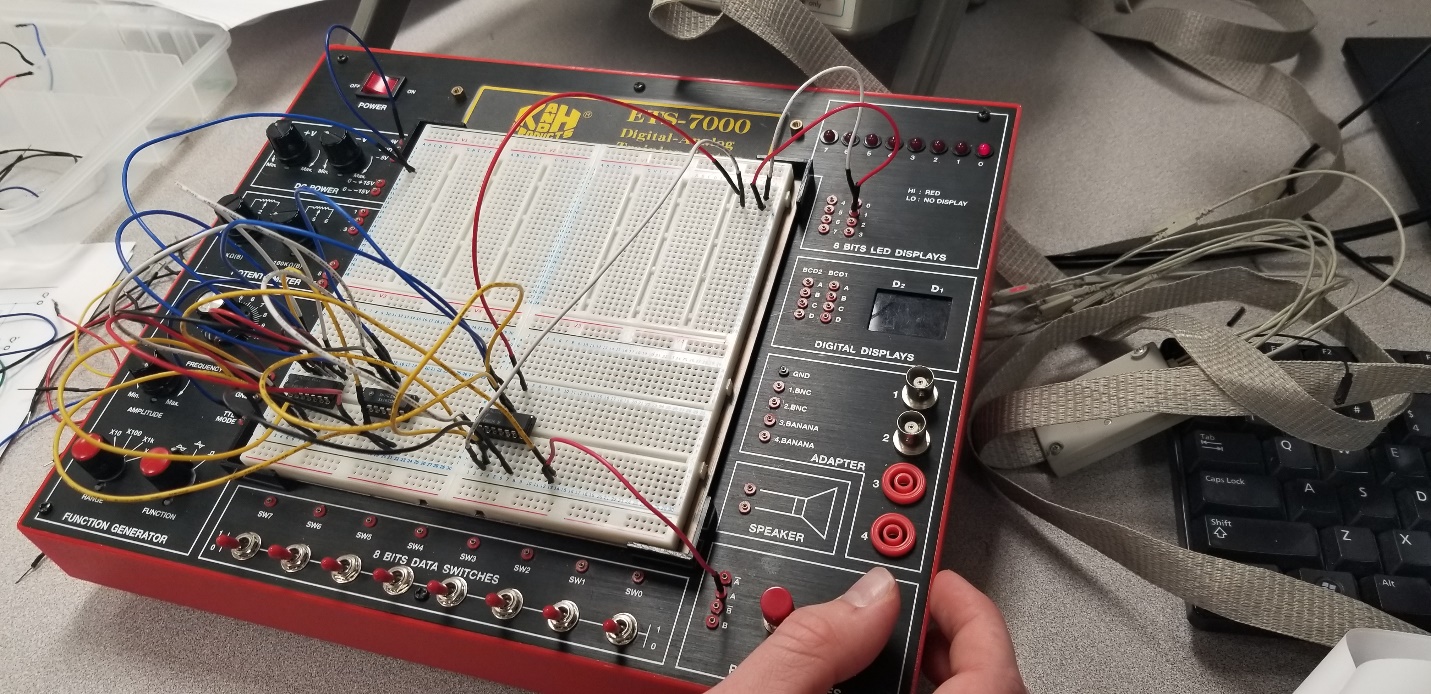
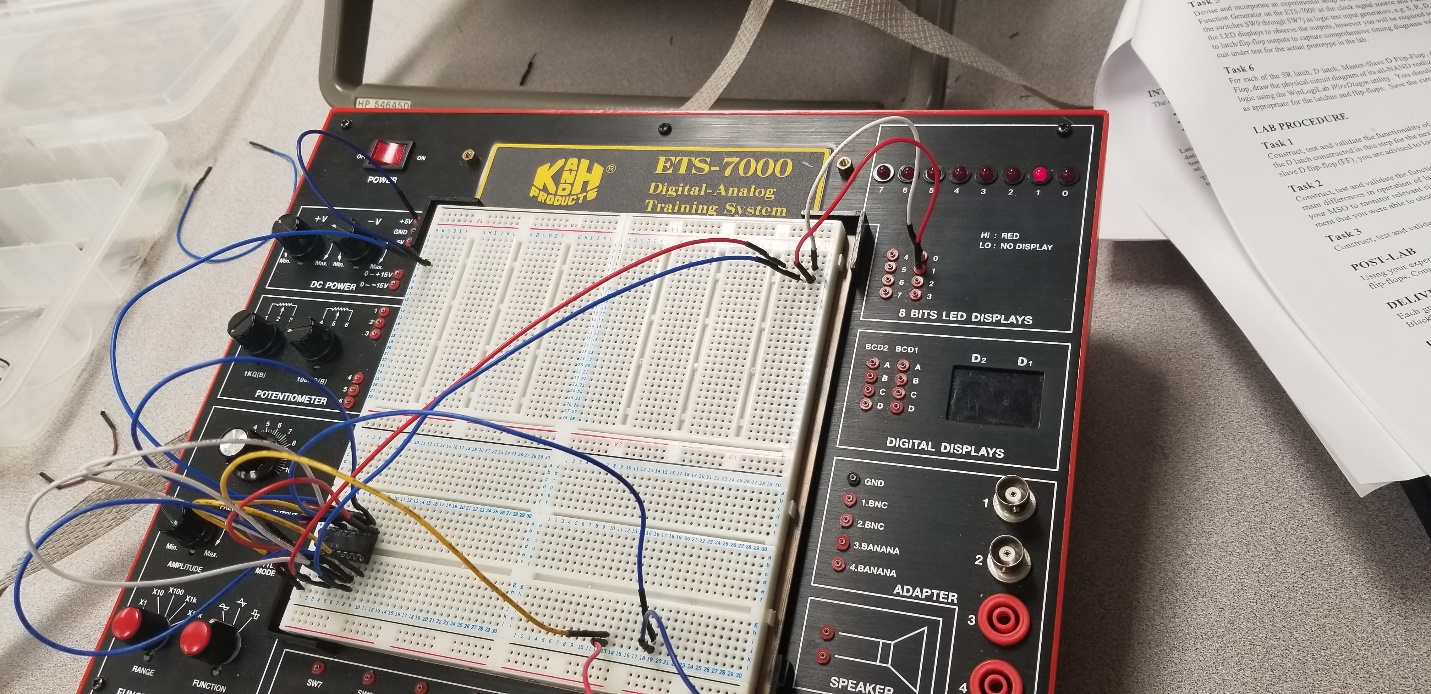
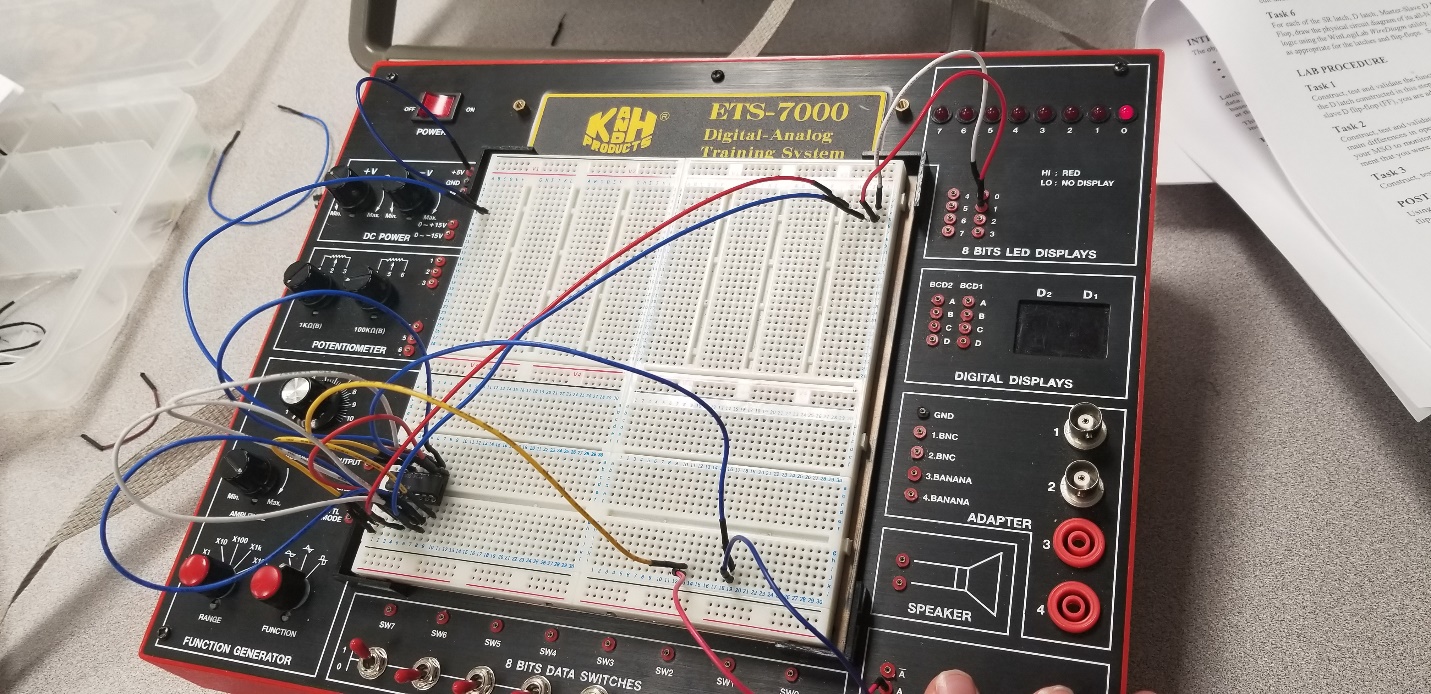


Fig 3 D-Latch Circuit



Discussion

In the Lab we were able to successfully create our D latch, master-slave D flip-flop, and an all-NAND D-type positive-edge-triggered flip-flop. The truth table all matched what we tested on each circuit.

Conclusion

This lab helped us understand how latches and flip-flops work. The circuits made matched our truth tables.

Appendix

Lab Attendance:              Bernard Owusu Sefah: Yes        Brandon Kowal: Yes

Involvement in Lab:                  Bernard Owusu Sefah: 55 Brandon Kowal: 45

Involvement in Lab Report:       Bernard Owusu Sefah: 60 Brandon Kowal: 40

POST LAB

    Latch: -

            The state transition of the latches starts as soon as the clock pulse changes to active state. The new state of the latch changes when the clock is in level 1 state only. This output is connected to the inputs of the latches through the combinational circuit. If the inputs applied to the latches change while clock is in level 1 state and the new state may occur. If the clock changes to level 0 then the new state will not occur. The problem is that it responds to a change in the level of clock pulse.

      Flipflop: -

          This circuit is operating when they are part of a sequential circuit that employs a common clock. The flipflop operates it to trigger it only during a signal transition. When a clock pulse goes through positive transition (from 0 to 1) it is defined as positive-edge-triggered, negative transition (from 1 to0) it is defined as negative-edge-triggered.

